Data Capture and Signal Processing (DCSP) Board

Data Capture and Signal Processing (DCSP) board is a VPX based conduction cooled card in 6U form factor. It employs high performance and high speed ADCs for digitizing the analog data, resource rich FPGA for performing operations such as decimation and TI's Keystone series DSPs for carrying out signal processing operations. The board is built as a lower power, light weight, single card replacement for Digitization card and Signal processing cards.

The DCSP board finds application in multiple airborne radar platforms:
- Exciter Receiver Processor
- Radar Processing Unit

KEY FEATURE
- Data acquisition, signal processing and DSP algorithms on the same platform
- Blind mate RF connection which mates to custom VPX Backplane.
- Two 16-bit Dual Channel ADCs sampling at 160MHz
- Time synchronously sampling at the four ADCs
- Remote FPGA programming support via LAN
- Board health monitoring over I2C interface
Interfaces

• sRIO interface: Two x4 sRIO Gen2 interfaces for communication through backplane for high-speed data transfer from DCSP card operating at 5 Gbps
• Two sFPDP interface operating at 2.5 Gbps through backplane for data transfer from DCSP board to external system
• Ethernet interface: Gigabit Ethernet switch on board provides connectivity among the processors, FPGA and other sub-systems through Front panel and back plane. The Microblaze based embedded sub-system implements the necessary software stack.

Software

• Control, Configuration and Status monitoring
  – MicroBlaze based embedded processor with peripherals such as boot memory, system monitor, timer module, UART, Interrupt controller etc. on Kintex-7 FPGA.
  – SYSBIOS is an advanced real-time operating system from Texas Instruments for use in a wide range of DSPs, ARMs, and microcontrollers. It is designed for use in embedded applications that need real-time scheduling, synchronization, and instrumentation. SYS/BIOS provides a wide range of system services such as:
    • Pre-emptive, deterministic multi-tasking
    • Hardware abstraction
    • Memory management
    • Configuration tools
    • Real-time
  – Exhaustive support for debug operations in the terms of counters, status registers etc.

Additional information

• 2GB DDR3 memory on Kintex-7 FPGA
• 2GB of DDR3 memory for each Keystone DSP Chip

FPGAs/Processor

• One Kintex-7 XC7K325T used for ADC interface and implementation of Signal processing functions.
• 2 instances of Keystone DSP TMS320C6674 with 4 cores each. Each chip provides a computational capability of 160 GMAC / 80 GFLOPs when operated at 1.25 GHz
• Two onboard 16-bit, 160 MSPS dual channel ADCs with Dynamic range 2.25Vp-p and 50 ohms impedance, each interfaced to Kintex FPGA.

ADC IF input

– SNR: SNR>70dBFS @Fin=70 MHz, Fs = 160 MHz
– SNR>68 dBFS @Fin=200 MHz, Fs = 160 MHz
– SFDR: SFDR>85dBFS @Fin=70 MHz, Fs = 160 MHz
– SFDR>75dBFS @Fin=200 MHz, Fs = 160 MHz
– ENOB: > 11.4 @Fin=70 MHz, Fs = 160 MHz
– 11.2 @Fin=160 MHz, Fs = 160 MHz

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MECHANICAL

• Conduction cooled 6U custom VPX form factor with Blind mate RF connection which mates to custom VPX Backplane.
• The board weighs 1.1 kg
**POWER CONSUMPTION**

- The board consumes a maximum of 55 W power
- Input voltages is 12V, 5V and 3.3V as per VPX standard

**ENVIRONMENTAL**

- Qualification
  - MIL-STD810D
  - EMI/EMC MIL-STD-461E
  - ESS: MIL-STD-2164 (EC)
- Temperature range
  - –40°C and +85°C (Storage)
  - –40°C and +55°C (Operational)