VPX Pulse Processor Boards

PRODUCT DESCRIPTION

The VPX Pulse Processor Boards are air-cooled boards in 6U VPX form factor which performs pulse processing algorithms on FPGA devices. It consists of two boards:

- Front IO board is a VPX board with two FPGA and dual-core processor
- Rear IO board (RTM) is connected through VPX backplane and is used for interfacing Optical transceivers, Gigabit Ethernet, LVTTI and RS42

The system receives optical data via SFPs on Rear IO board and passes on to Virtex 6 FPGA on Front IO board across VPX backplane connector. The processed data is sent to Virtex-5 FPGA through MGT copper links on the board, using Aurora protocol. The processed data is sent to the dual core MPC8640D processor for further processing and it is sent over Ethernet to external system.

The board finds application in electronic warfare systems.

KEY FEATURES

- Pulse processing on FPGAs
- Dual-core Processor MPC8640D for processing software algorithms
  - MPC8640D is interfaced to Virtex-5 FPGA via sRIO and PCIe links
- Supports x1 lane PCIe interface to backplane
- Capable of operating as standalone SBC
- Front IO board
  - Supports data transfer on the VME bus over VPX @ > 50 MBytes per second
  - Two independent banks of 36-bit QDR II interface, each having 2M x4x 36bits
  - Two independent banks 32-bit DDR, each having 128 MBytes size
- Rear IO board
  - One 10/100/1000 Ethernet interface
  - Four optical serial links, each supporting 3.125 Gbps serial data rate
  - 16 RS422 Transmitter and 16 RS422 Receiver ports on Micro-D connectors
  - 32 TTL IO interfaces on Micro-D connector

SPECIFICATIONS

FPGAs / Processor

- Virtex-5 FX100T FPGA with Embedded PowerPC440 Embedded Processor
- Virtex-6 LX240T FPGA
- Dual core processor MPC8640D
Interfaces
- Six SFP optical data ports, two from front, four from Rear IO board
- Three Ethernet ports; two on Front IO board and one on Rear IO board
- 16 RS422 Transmitters & 16 RS422 Receivers, 32 TTL IOs
- Master slave communication with other SBCs over
  - x1 lane PCIe interface
  - SRIO
- Inter-FPGA MGT links (data transfer speed up to 3.125 Gbps)
- JTAG, RS232 access from Rear IO board
- VME 2esst interface to SBC

Software / IP
- Diagnostic RTL for validation of board
- Linux Operating system on dual-core MPC8640D

Expansion Slots
- PMC Slot

Additional Information
- 1 GB DDR2 SDRAM (2 x 128M x 16 x 2 Banks) for MPC8640D
- 32 MB NOR Flash each for Virtex-5 Configuration, Virtex-5 software, Virtex-6 Configuration and MPC8640D

MECHANICAL
- Air cooled 6U VPX board

POWER CONSUMPTION
- The unit consumes 70W
- Input voltage is 12V, 5V and 3.3V

ENVIRONMENTAL
- Qualification: 168 hours endurance test (Operational)
- Temperature range: −40°C and +85°C (Storage)
- −40°C and +55°C (Operational)

PART NUMBER(S)

| CH1090  | VPX Pulse Processor Boards |