High Speed Data Acquisition Board

PRODUCT DESCRIPTION

The High Speed Data Acquisition Board has onboard ADCs and FPGAs which can be used for data acquisition as well as DSP processing. The board is of 6U dimension featuring hybrid VME-VXS interfaces for high speed backplane communication. The air-cooled board has Ethernet links and RocketIO links for data communication.

The board is used in data acquisition and processing system in electronic warfare application. This board is used in radar characterization and identification system.

KEY FEATURES

- High speed data acquisition capability with 12-bit ADC at 1333 Msp
- Onboard clock generation for ADC sampling with programmability for: 1333, 500, 666 and 125 Msp
- 256 point FFT calculation in real time in Virtex-6 FPGA to validate trigger in frequency domain
- Programmable Pre-trigger and Post-trigger samples in steps of 4 samples
- Two trigger modes supported: programmable internal and external trigger
- Time of arrival resolution of 8ns for internal trigger and 2.5ns for external trigger
- Dead time of less than 400ns between two triggers
- Signal conditioning card providing BPF and LPF filtering for all channels
- Windows based GUI application with supported APIs for sending commands to card through Ethernet, VME

SPECIFICATIONS

FPGAs / Processor / ADC

- Virtex-6 SX315T FPGA for ADC data capture and processing
- Virtex-5 FX100T with PowerPC440 Embedded Processor for control and communication
- Two 12-bit dual channel ADCs providing a total of 4 analog input channels
  - Input signal in the range of -40dBm to 10dBm supported on each channel
  - Configurable to either 3.6 Gsps interleaved or 1.8 Gsps dual ADC
  - SFDR more than 58dBFS and SNR more than 50dBFS

Interfaces

- 8 RocketIO to backplane - VITA 41 (VXS connector)
- 2 RocketIO to front panel - Infiniband connector
- 64-bit VME interface to backplane - VME P1 and P2
- 7 SMA Connector on front panel - 4 for analog input, 1 for external trigger, 1 for external clock and 1 for BITE out
- 32 debug I/Os to rear panel
- 2 UART interfaces (1 per FPGA) to backplane
- 1 Gigabit Ethernet to front panel - RJ45 connector
- JTAG interface for FPGA programming on front panel
- API support for transferring captured data through Ethernet, VME or VXS link
- Built-in self tests to check the health status of the card
- Input signal amplitude upto 18dBm (5V peak to peak)

Software / IP

- MicroBlaze, on Virtex-6 FPGA executing standalone software in interrupt mode
- Linux is running on PowerPC440 of Virtex-5 FPGA for interpreting commands
- Windows based GUI application with supported APIs for sending commands to card through Ethernet and VME

Expansion Slots

- Mezzanine card for signal conditioning
  - Signal Conditioning card provide 140-180 MHz BPF, 750-1250 MHz BPF or DC-2 GHz LPF filtering options of all four channels
- CASPS

Enabling Excellence
**Additional Information**
- 2 banks of 64-bit wide 1 GB DDR3 and 16 MB SPI flash interfaced to Virtex-6 FPGA
- 1 GB 64-bit wide DDR2, 32-bit wide 512 MB DDR2 and 128 MB NOR flash interfaced to Virtex-5 FPGA

**MECHANICAL**
- Air cooled board in 6U VME-VXS form factor
- The board weighs < 900 grams

**POWER CONSUMPTION**
- Total power consumption of less than 70W

**ENVIRONMENTAL**
- Qualification: Environmental (JSS 55555 standard): Thermal cycling, random vibration, damp heat & altitude test
  EMI/EMC: MIL-STD-461E
- Temperature range: −20°C and +70°C (Storage)  
  −10°C and +55°C (Operational)

**PART NUMBER(S)**
The following variants of this board are available:

<table>
<thead>
<tr>
<th>Part Numbers</th>
<th>Variants</th>
<th>Features</th>
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| CB10B0       | Variant 1 (defined above) | • Dual FPGA architecture: Virtex-6 SX315T and Virtex-5 FX100T  
• 4 analog channels  
• Two dual channel ADC: 12-bit ADC @ 1333 Msp  
(capable of operating as single channel 12-bit ADC @ 2666 Msp)  
• Air-cooled board |
| CB10B1       | Variant 2 | • Dual FPGA architecture: Virtex-6 SX315T and Virtex-5 FX100T  
• 4 analog channels  
  • One dual channel ADC: 8-bit ADC @ 1333 Msp  
  (capable of operating as single channel 8-bit ADC @ 2666 Msp)  
  • One dual channel ADC: 10-bit ADC @ 1333 Msp  
  (capable of operating as single channel ADC @ 2666 Msp)  
• Air-cooled board |
| CB10B2       | Variant 3 | • Single FPGA Architecture: Virtex-6 SX315T  
• Only one dual channel 12-bit ADC sampling @ 1333 Msp  
(capable of operating as single channel ADC @ 2666 Msp)  
• External clock supported for ADC sampling  
• Designed for air cooled and conduction cooled form factor  
• RTL intelligence to determine end of pulse and to calculate pulse width |