Quad Digital Receiver (QDR) Board

PRODUCT DESCRIPTION

The Quad Digital Receiver (QDR) Board is a 6U conduction cooled board with VPX connector for backplane interfacing. The board has four high speed ADCs capable of sampling RF signals synchronously. The board has FPGAs to implement signal processing algorithms. IF front-end module with 1 GHz bandpass filter and amplifier for signal conditioning. Supports data transfer, configuration and remote updation of firmware over Gigabit Ethernet interface.

The board is used for RF signal acquisition and processing in electronic warfare systems.

KEY FEATURES

- Synchronous sampling from four ADC channels
- Phase synchronization of $\leq 3$ degrees
- Analog input bandwidth: 1.5 GHz to 2.5 GHz sampled at 2.7 Gsps
- Provision for ADC clocking through onboard clock or external input
- Dedicated signal conditioning front end module
  - Bandpass filter and amplifier to enhance the RF signal power
- 512 point FFT engine and Cordic algorithm for processing ADC data
- Remote FPGA image upgrade
- Graphical user interface support for
  - Configuring of onboard devices
  - Capturing of data
  - Measuring of phase, amplitude and frequency of the captured data
  - Health monitoring of board and device
  - Signal generator control using SCIPI command for automatic testing

SPECIFICATIONS

FPGAs / Processor / ADC

- Four 12-bit ADCs connected in DES mode aggregating to four channel input sampling at 2.7 Gsps
- Two Xilinx Virtex-6 SX475T FPGAs for signal processing
- One Xilinx Virtex-6 LX240T FPGA for control
- MicroBlaze based embedded sub-system on FPGA

Interfaces

- Gigabit Ethernet over RJ-45 connector
- External clock input over SMA connector
- 96 LVTTL interface terminated on the backplane
- 4 lane RocketIO interface from each signal processing FPGA terminated on backplane for high speed data transfer (10G)
- VPX backplane connectivity
Software / IP
- Linux Operating System on control FPGA
- Standalone application on signal processing FPGA for control and health monitoring
- Multiple signal processing algorithms running on FPGAs
- Graphical user interface support for
  - Configuring of onboard devices
  - Capturing of data
  - Measuring of phase, amplitude and frequency of the captured data
  - Health monitoring of board and device
- RTL & software for board validation

MECHANICAL
- Conduction-cooled 6U board with VPX connectors
  - Compatible to air-cooled chassis
- The system weighs 1.23 kg (2.2 kg with IF front-end module)

POWER CONSUMPTION
- The unit consumes < 72W
- Input voltage is 12V and 5V over VPX connector

ENVIRONMENTAL
- Qualification: JSS 55555
  MIL-STD-461E
- Temperature range: -40°C and +85°C (Storage)
  -40°C and +55°C (Operational)

PART NUMBER(S)

| CB1060 | Quad Digital Receiver (QDR) Board |