High Speed FFT based Pulse Detection for a Digital ESM Receiver for Airborne Applications

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Abstract:

This paper brings out a unique FFT based Pulse detection approach for a Two channel Digital ESM (Electronic Support Measure) Receiver targeted for Airborne EW applications. The proposed approach uses a high speed ADC (1.5 GHz) and FPGA based architecture for sampling and Digital processing of the received signals. A high speed 256 point FFT engine is realised in FPGA to separate up to 4 overlapped pulses in 500 MHz instantaneous BW. Pulses with PW as low as 100 ns can be detected in presence of CW signals in the 750-1250 MHz input band with this approach. The hardware realised to verify the algorithm and the FPGA implementation for Pulse Detection Engine are discussed in the paper. The simulated and measured results for the Pulse Detection algorithm are presented. This pulse detection approach gives up to 45 dB single signal dynamic range.

Keywords: EW, ESM, Digital Receiver, LPI, POI, DIFM, ADC, FFT, Peak Detection, FPGA, High Speed Design, PCB, Signal integrity.

I. INTRODUCTION

ESM Receivers function to search, intercept, locate and identify sources of enemy Electromagnetic radiation. The information they produce is used for the purpose of threat recognition and for the tactical deployment of military forces or assets such as ECM equipment. As the EW scenario is becoming dense day by day, the ESM Receivers are required to process a few million pulses/second for maintaining a high POI (Probability of Intercept). Earlier ESM Receivers have employed analog DIFM (Digital Instantaneous Frequency Measurement) techniques for frequency measurement. DIFM Receivers can only measure a single signal at a time and have a limited pulse processing capability.

The EW scenario today has become very dense and the radar frequency spectrum has become very crowded. Today, many types of Radar are operating very close in frequency range with their signals overlapping in time domain. Hence detection of overlapped pulses and LPI waveforms in presence of noise are the new requirements emerging for ESM Receiver Design.

The lack of *a priori* knowledge about the waveform of interest makes the design of modern Digital ESM Receiver very challenging. Also the noise energy which occupies the same portion of the frequency spectrum as the signal complicates the matter even further. [1]

The availability of high speed ADCs in the GHz range have made direct sampling of signals possible in the IF range. Emergence of high density/high speed FPGAs with dedicated resources for performing DSP operations has enabled implementation of ESM techniques operating in real time.

An ADC-FPGA based signal processing architecture was described in [4] for Digital Receiver using FFT (Fast Fourier Transform) at low frequency. It presented results for frequency measurement of a100 ns pulse using a Xilinx Logic Core FFT IP for performing 256 point FFT. The Xilinx FFT core has latency in order of µs when configured for 256 point FFT operation. In order to interface with high speed ADC, multiple Xilinx FFT cores have to be used in parallel to achieve the complete throughput without the loss of any input samples. The current paper describes a high speed FFT IP performing 256 point FFT in less than 200 ns which can work with high speed ADC data and is completely pipelined.

II. PULSE DETECTION ARCHITECTURE

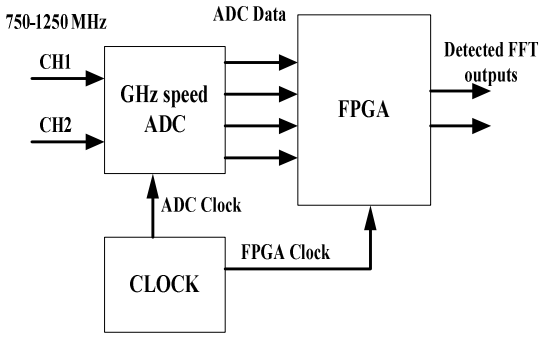

Fig.1: Pulse Detection Architecture for Digital ESM Receiver

The Pulse Detection Architecture is shown in Fig.1

In this architecture, high speed ADC converts the incoming signals to Digital domain and FPGA acts as the signal processing device. The selected ADC is a two channel Device.

1. Selection of ADC sampling frequency: In the proposed approach, Band pass sampling theorem is used for sampling two channels in 750-1250 MHz band. Band pass sampling allows working with a lower sampling frequency and a single two channel ADC. This saves space and power and also simplifies Hardware design. The ADC sampling frequency (Fs) is selected close to 1500 MHz as per the Band pass sampling criteria given below

$$\frac{2Fc-B}{m} \geq Fs \geq \frac{2Fc+B}{m+1} \qquad \ldots(1)$$

Where
m- Any positive integer so that Fs ≥ 2B
Fc- Center Frequency
Fs- Sampling frequency
B- Input BW
For our case,
Fc = 1GHz
B = 500 MHz
For m =1, equation (1) gives
1500 MHz ≥ *Fs* ≥ 1250 MHz

So For Band pass sampling criteria to be fulfilled, Sampling frequency (*Fs*) can be any frequency between 1250 to 1500 MHz.

Each RF signal in the 750-1250 MHz band is sampled at 1350 MHz. Hence spectrum folding is observed at the ADC output due to band pass sampling. The folding takes place at 675 MHz (Fs/2). Hence 750 MHz signal at ADC input becomes 600 MHz (1350-750) at ADC output where as 1250 MHz at ADC input becomes 100 MHz (1350-1250). So input to FFT module is a bandpass signal from 100-600 MHz. Folding is not a problem as the mapping of frequency is one to one as we are following the Band pass sampling theorem.

2. Selection of number of points of FFT: The selection of number of points of FFT depends on a number of factors. The frequency resolution desired at the FFT output, ADC sampling frequency, ease of Real time implementation and the minimum pulse width to be processed. In order to process a minimum Pulse width of 100 ns, the data window to be processed should not be more than twice the PW otherwise the performance of FFT degrades. Hence the data frame of FFT should not be more than 200 ns. Ideally one would like to have the entire FFT frame filled with the data for optimum FFT results. For an ADC sampling frequency of 1.5 GHz, selection of N=256 gives a frequency resolution of 5.86 MHz (1.5 GHz/256) at the FFT output and a data window of 170 ns (256/1.5 GHz). Hence N=256 is selected for Pulse Detection approach.

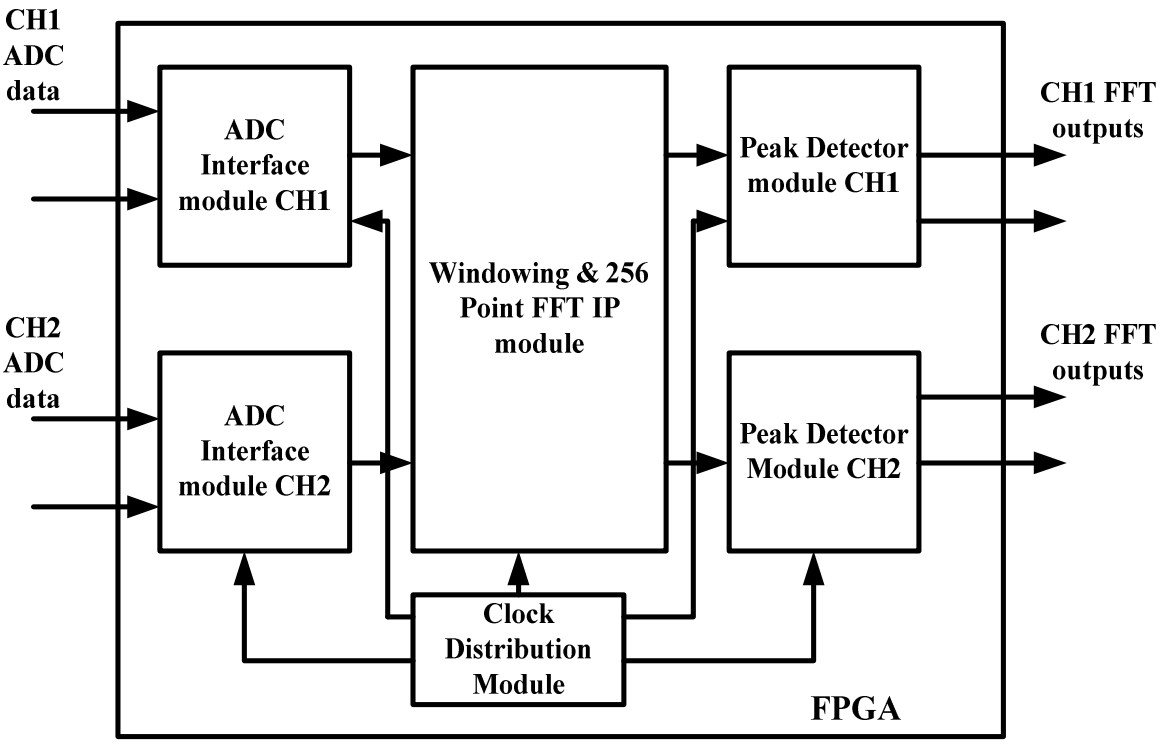

Fig. 2: FPGA Based Signal Processing architecture

III. FPGA BASED SIGNAL PROCESSING ARCHITECTURE

The FPGA signal processing architecture is shown in Fig 2. It consists of the following main modules

1. ***ADC interface module:*** The ADC Interface module captures the data from the dual channel ADC operating at 337.5 MHz (Fs/4) Double Data Rate and stores them in the FPGA Block RAMs for further processing. The differential data coming from the ADC is latched with the help of source synchronous clock from the ADC. The data is converted to single ended format using FPGA input buffers. The ADC data format is offset binary. The data is converted into two's complement format and given to the FFT module. Two such modules are instantiated in order to capture two channels of ADC data. The ADC interface module generates the control signals for the ADC and also for power-on and on demand calibration.

2. ***256 point FFT module:*** Fast Fourier Transform (FFT) is an efficient algorithm to compute the Discrete Fourier Transform (DFT).The DFT function transforms the time domain representation of a signal into its frequency domain representation. The 256 point FFT engine makes use of Radix-4 butterfly structure for the computation of the FFT. In order to achieve faster performance, two instances of Radix-4 butterflies are instantiated at each stage. Each of the Radix-4 butterflies accepts four samples for processing at a time. For a N point FFT, the process is carried out in stages, where the number of stages is equal to $\log_4 N$.The current design calculates the 256 point FFT - thus having $\log_4 256 = 4$ stages. Since the time domain sampled inputs from ADC contain only the real values, data from two channels can be fed as real and imaginary data to a single FFT IP. The algorithm explained in [2],of performing Two N-point Real FFTs using one complex N point FFT is made use of to achieve the functionality. Since the FFT is symmetric for input data of this nature, the final stage outputs only the first 128 bin values. The resolution of the FFT engine is fs/N, where fs is the sampling frequency at which the input is sampled. The FFT operation is performed on every incoming sample and is a continuous operation. The input samples to the FFT IP are not overlapped to keep processing to a minimum considering real time implementation. The samples are windowed prior to the FFT operation to reduce the side lobe leakage. A Kaiser window is used with $\beta = 3$. Of all the windows, Kaiser Window is selected because it has good main lobe width and sidelobe attenuation. [5]

3. ***Peak Detector module:*** A peak detector module is designed for extracting peak from FFT outputs. Two such modules are used for the two channel FFT outputs. Peak Detector Module receives four FFT output samples on every clock. A FFT output frame consists of 128 samples. For peak detection, data needs to be processed serially. Hence an intermediate buffer is used to store the incoming data. Writing of a frame requires 32 cycles, while processing requires 128 clocks. Hence there are 4 instances of processing elements. Peak detection process begins only if there are at least four complete frames of data. Side lobe rejection considerations are taken into account while detecting peaks. The DFT leakage is already minimised by applying Window function to the incoming data before the calculation of the FFT. A fixed threshold is set in the peak detector module above which a candidate bin is checked for peak detection criteria.

4. ***Clock Distribution module:*** Clock distribution module is used to generate and distribute clocks to every module of FPGA. All the external clocks coming to the FPGA are passed through Digital Clock Managers (DCM) for efficient use of Clock structures available in FPGA. All the clock paths are covered by timing constraints to get optimum performance. The Divide by Eight clock derived from the ADC sampling clock is used as the core processing clock in FPGA.

IV. SIMULATION RESULTS

The FPGA pulse detection design was simulated to verify the functionality. The simulation was done using Modelsim software by ModelTech. Extensive simulation has been carried out with real world data. The data was generated in MATLAB for sampling frequency of 1350 MHz and scaled to the ADC voltage output. The data format used was offset binary as per the selected ADC. The Fig 3 shows the peak detector module output

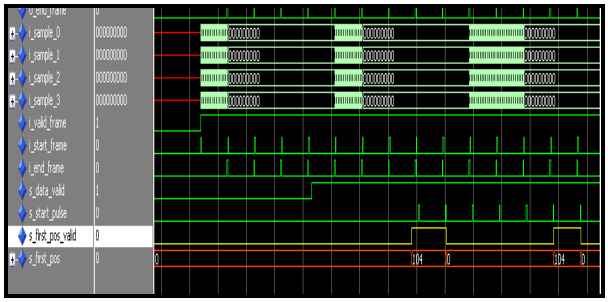

Fig. 3. Peak Detector module output for 800 MHz 100 ns Pulse

The simulation shows the detected FFT bin at the peak detector module output. The detected bin position is 104 which corresponds to a folded frequency of 548.4375 MHz (Measured as 1350-548.4375=801.5625 MHz) at the sampling frequency of 1350 MHz

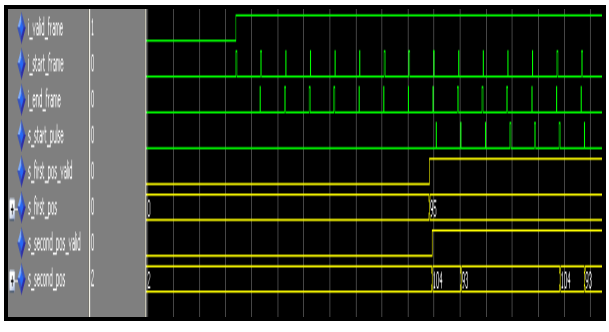

Fig. 4. Peak Detector output for 800 MHz 100 ns Pulse overlapped with 850 MHz CW case

Figure 4 shows peak detector module output for two signal case. The detected bin positions are 104 and 95 corresponding to measured frequencies of 801.5625 MHz and 849.0235 MHz respectively

V. HARDWARE IMPLEMENTATION

To validate the Pulse detection algorithm, a Xilinx Virtex-4 LX 100 FPGA based hardware platform with a high speed Two channel 1.5 GHz ADC was designed. The hardware has a facility of using either the external as well as internal clock. The FPGA processing clock is derived from the ADC sampling clock using an on board Clock Divider chip. It has two high speed SRAMs for data storage. The ADC captured data can be stored in these memories for further processing. Signal integrity analysis for critical traces on the Printed Circuit Board has been performed which include ADC input circuitry, ADC-FPGA data interfaces, ADC-SRAM interface, internal as well as external clock paths etc. Due care has been taken to match the traces for impedance, length and skew within tolerable limits. High speed Design guidelines have been followed while designing the hardware

Number of layers – 18
Material – FR4
Controlled Impedance – Yes

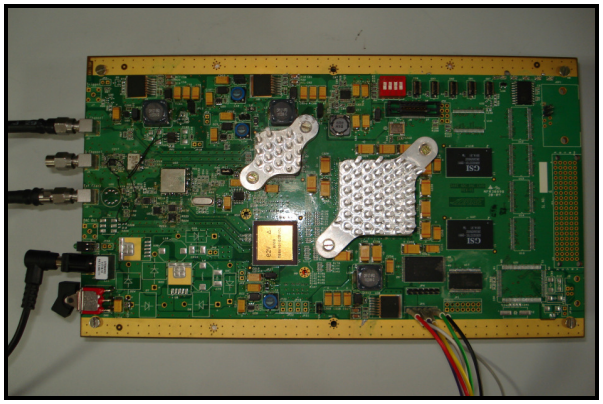

Fig.5 Digital Receiver Hardware

The board has been tested for sampling frequency of operation up to 1.5 GHz

VI. TEST RESULTS

Pulsed analog signal generators from Agilent were used to generate pulsed RF signals and external clock for the board. The sampling frequency was set to 1 GHz. The Peak Detector module outputs were observed on Logic Analyzer as well as Xilinx Chipscope Pro (Hardware Debugger). For pulse on pulse frequency measurement, two synchronized pulsed analog signal generators were used. Their pulsed RF outputs were combined using a Mini Circuit power combiner (10-2500 MHz) and given to ADC. The ADC data integrity was tested by capturing ADC output data buses in Xilinx Chipscope Pro and analyzing it in MATLAB. The complete Pulse Detection algorithm was written in VHDL and downloaded on the board using Xilinx IMPACT tool. .

1. Pulse over Pulse signal condition: Two synchronized pulsed signals of frequency 750 MHz (PW = 400 ns, PRI= 2 µs, Power = -15 dBm) and 800MHz (PW = 100 ns, PRI = 1 µs, Power = -5 dBm) were combined and given to the hardware. The Peak detector module reported FFT bin of 51 and 64 which correspond to a folded frequency of 199.22 MHz (Measured Frequency of 800.78 MHz) and 250 MHz (Measured frequency of 750 MHz). The Xilinx Chipscope Output and the MATLAB FFT output for this case are shown in Fig 6 and 7 respectively.

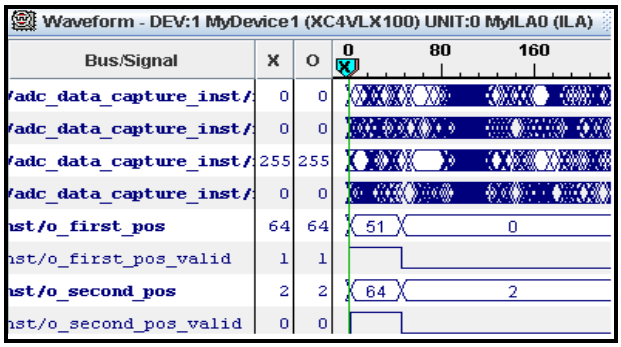

Fig 6 Xilinx Chipscope Pro output Pulse over Pulse signal case

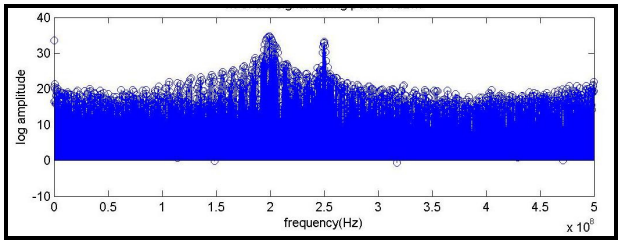

Fig 7 MATLAB FFT output for pulse over pulse signal case

2. CW over Pulse signal condition: One CW signal of frequency 850 MHz (Power = 0 dBm) and a pulsed signal of frequency 750 MHz (PW = 100 ns, PRI = 2 µs, Power = -15 dBm) were combined and given to the Digital Receiver hardware. The Peak detector module reported FFT bin of 38 and 64 which correspond to a folded frequency of 148.43 MHz (Measured Frequency of 851..57 MHz) and 250 MHz (Measured frequency of 750 MHz). The Xilinx Chipscope Output and the MATLAB FFT output for this case are shown in Fig 8 and 9 respectively.

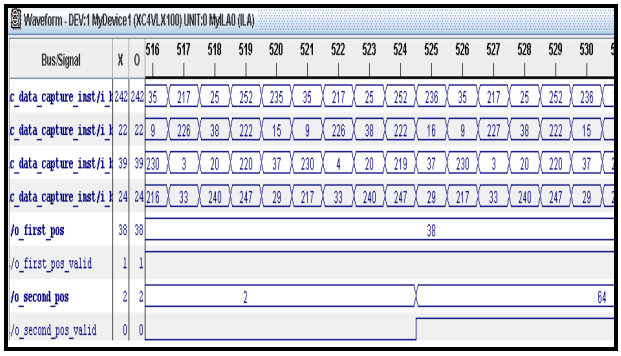

Fig 8 Xilinx Chipscope Pro output for CW over pulse case

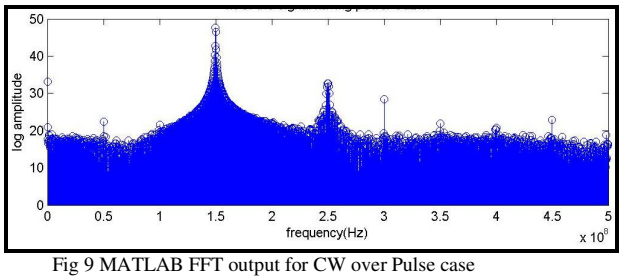

Fig 9 MATLAB FFT output for CW over Pulse case

3. ***FPGA Resource Utilization:*** Table 1 shows the FPGA resource utilization for the pulse Detection algorithm using Xilinx Virtex-4 LX 100 FPGA.

TABLE 1

Number of Slices	12,475
Number of Block RAMs	98
Number of DCMs	2
Number of DSP Slices	96

VII. CONCLUSION

From the limited data collected, it is observed that the proposed pulse detection approach can directly sample and process two simultaneous signals and can measure frequency of a 100 ns pulse in the 750-1250 MHz frequency band. The result for Pulse over Pulse signal condition and CW over pulse signal condition was also presented. A single signal dynamic range of 45 dB was obtained using the current approach. The overall performance can only be obtained when the algorithms are tested with the complete Digital ESM Receiver setup and Pulse Descriptor Words are generated corresponding to every pulse received. Some topics of further investigation are setting of threshold for two signal cases, extending the detection problem to three signal and four signal cases and setting of adaptive threshold.

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REFERENCES

[1] James B.Y. Tsui, *Digital Techniques for wideband Receivers,* 2nd ed. Norwood, MA: Artech house, 2001.

[2] Richard Lyons, *Understanding Digital Signal Processing,* Pearson Education, 2004.

[3] Richard G. Wiley, *ELINT The interception and Analysis of Radar Signals,* Norwood, MA: Artech House, 2006.

[4] Abhijit Kulkarni, Virendra Kr. Jaiswal, Girish M, Priya Suresh N and Dr U.K.Revankar, " High Speed Digital Processing for EW Receiver applications", *Proc, Int. Symposium on Microwaves*, Dec 2008, vol. 1, pp. 121-125.

[5] Fredric J Harris, "On the use of Windows for harmonic Analysis with the Discrete Fourier Transform", *Proc. Of IEEE*, Vol. 66, No. 1, Jan 1978.

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