FPGA based Implementation of Baseband Generator for RADAR Applications

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***Abstract*- Performance of any RADAR system deployed in Electronic Counter Measure applications is significantly enhanced when it has the capability to generate various types of signal waveforms on-the-fly with the least changeover time. The signal can either be generated at Intermediate Frequency (IF) directly or using the base-band components, which are combined to form the IF signal. Some of the types of waveforms typically generated are continuous wave, frequency modulated, amplitude modulated or sweep signals. This paper emphasizes on the generation of waveforms digitally using Field Programmable Gate Arrays (FPGA's), and at the same time converting digital signals to analog signals on-board using ultra high speed Digital to Analog converter (DAC) operating at speeds up to 2 GSPS. System-on-chip concept is used by implementing soft processor core "MicroBlaze" on Xilinx FPGA, thereby reducing component count on the board and thereby design's complexity. This paper also focuses on the high-speed mixed signal design aspects as traditional methods of board layout techniques no longer work at GHz speeds. A comparison of the DAC datasheet specifications and real-time results is provided to show how mixed signal design techniques helped to achieve a close match.**

***Key Words*- FPGA, PCB design techniques for high speed ADC/DAC and RF, Configurable Waveform Generation, AM, FM, Scalability, CPWG, SFDR, Phase Noise**

I. INTRODUCTION

Generation of the appropriate base band signal waveform is an important parameter for stationary radars or Electronic Counter Measure (ECM) radars. In previous generation of radars transmitted waveforms were generated in the analog domain [2]. Likewise, receive signal processing was also carried out in the Analog domain. Modern radars perform up-conversion, down-conversion, and receive signal processing functions in the digital domain. Processing in the digital domain significantly reduces design complexities of analog domain, provides programmable options, and enhances design scalability. With the technological advancements, sampling rates of high speed DAC's are moving northwards, which require processing of digital data at very high clock rates. Modern day high-density Field Programmable Gate Array (FPGAs) are best suited for such applications as they provide very high computational bandwidth. Also, the latest technology demands need for a quicker reaction to an action, such as Electronic Counter Measure in the Electronic Warfare. FPGAs can implement time-critical events in real time, thereby enabling a faster response. Baseband Generator enables generation of a wide variety of waveforms based on the commands received from a companion sub-system or a user friendly GUI implemented on a host controller PC. The frequency of the generated waveform is in the range of 2 MHz to 600 MHz. In this paper, we present the (FPGA) based implementation of Baseband Generator for Electronic Counter Measure applications.

II. SYSTEM DESCRIPTION

Top level architecture of the Baseband Generator is depicted in Figure 1. Baseband generator essentially consists of 3 key components – FPGA and DAC based hardware platform, RTL implemented on Virtex-5 FPGA, and software running on the MicroBlaze processor core. Additionally, user-friendly GUI is implemented on a host controller PC, which sends commands to the MicroBlaze processor over Ethernet interface, and as well receives periodic updates from the MicroBlaze. Details of the GUI are not in the scope of this paper.

III. HARDWARE PLATFORM

Hardware platform broadly consists of a single 2 GSPS, 12-bit DAC from Teledyne, Virtex-5 FPGA from Xilinx, GigE Ethernet link, clock generation circuitry, voltage regulators, on-board debug components, and power monitor and temperature monitor circuits. An EEPROM is provided to store design specific information such as Ethernet MAC ID, hardware version, software version and RTL version. A low speed ADC input interface is provided to supply a modulating signal. Baseband generator digitizes this analog input and uses this information to generate an AM or FM modulated signal. Platform Flash is provided for storing FPGA programming file. Clock for the DAC operation needs to be stable. Therefore an external OCXO supplies 100 MHz reference clock to the on-board clock synthesizer having integrated VCO. Reference clock is fed to the hardware platform via SMA connector interface. An optical link interface capable of operating up to 3.125 Gbps data rates is provided for future scalability. The data received over this link can be transferred over the high speed DAC interface transparently or after carrying out digital signal processing in the FPGA. Baseband generator can act as a Jamming Unit by receiving data from radar receiver via this high speed serial optical link and transmitting mirrored copy over the DAC.

Based on the hardware features discussed above, CoreEL has realized a baseband generator module capable of generating Multiple Carriers, Modulated signals, Modulating

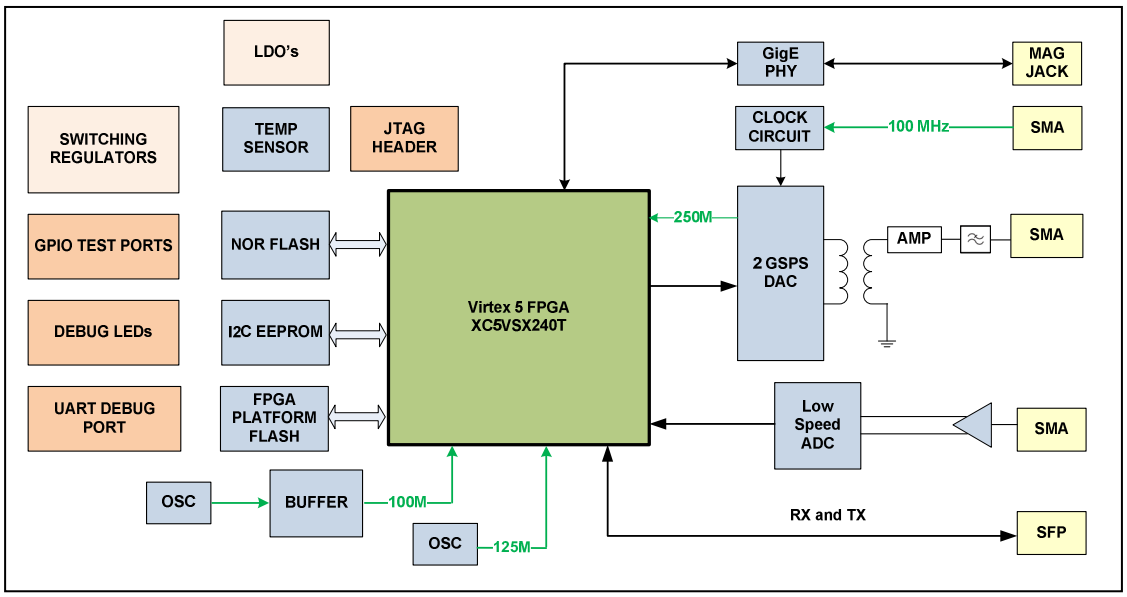

Figure 1: Base-band Generator top-level Architecture

signals and Sweep signals up to 600 MHz. DAC performance on this hardware platform is very close to its Datasheet specifications as PCB design techniques for high speed ADC / DAC and RF signals are strictly followed.

IV. BASE-BAND GENERATOR RTL

Figure 2 shows the RTL implementation of Based-band Generator.

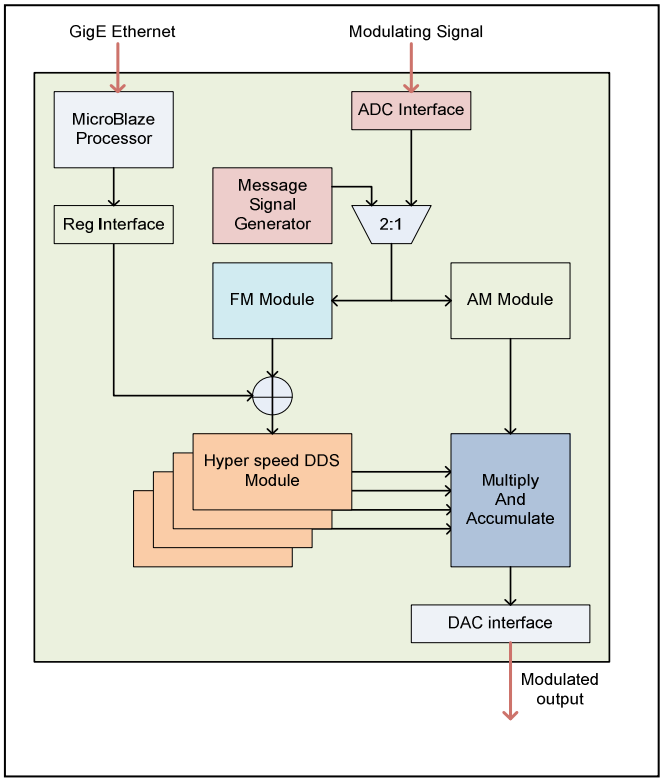

Figure 2: Baseband Generator RTL Block Diagram

It is a signal generator capable of generating Carrier Wave or Modulated signal in the output frequency range of 2 MHz to 600 MHz. RTL design consists of following sub modules.

MicroBlaze processor, the embedded sub-system module accepts commands from the host controller through GigE Ethernet interface and configures appropriate registers to generate the user selected waveform.

Register interface module contains a set of registers classified as – control registers (R/W) which can be read or written by the processor, and status registers (read only) which are set by the RTL logic and can be read only by the processor.

ADC interface accepts the sampled ADC data from the external low-speed ADC chip and the sampled values are used as modulating signal to generate AM/FM data.

Message signal generator consists of a look-up-table (LUT) that stores the data samples corresponding to a modulating signal. This LUT is initialized by the embedded sub-system as per the data provided by the host controller. As an alternate option to the ADC samples, data from the look-up-table can be read and provided as modulating signal to AM/FM.

AM module provides the Modulating signal data samples to the MAC (Multiplier and Accumulator) for generating AM modulated signal. The AM modulating data can be selected either from the LUT or an external ADC interface based on the command received from the host controller. Modulation index / depth can also be programmed for the AM module.

FM module is used to select the Frequency deviation based on the selected Modulating signal frequency. A range of frequency deviations can be supported.

Hyper-speed DDS block implements the Direct Digital Synthesis (DDS) functionality. It consists of 2-modules namely phase accumulator and ROM bank. The phase accumulator module generates the phase addresses based on the received Frequency Tuning Words (FTW) and provides

them as an address to ROM bank. The ROM bank provides the data samples corresponding to the phase address provided.

Multiply and Accumulate engine multiplies the generated carrier wave from the DDS with the modulating signal provided by the AM module in case of AM modulation. All the DDS output frequencies are added together by the Accumulator in case of multi-carrier generation. Scaling logic is also implemented as part of this engine.

DAC interface provides digital samples corresponding to the user selected baseband frequency to the on-board DAC at a rate of 250 MHz LVDS DDR. Data format supported is offset binary.

Due to the constraints posed by high speed DAC, RTL design is pipelined sufficiently to meet the timing closure requirements within the FPGA.

V. Base-Band Generator Software

Xilinx's series of FPGAs provide the flexibility of implementing soft processor core "MicroBlaze" [4] using the Xilinx Embedded development Kit (EDK). These embedded processors are seamlessly integrated with other essential components of an embedded sub-system such as Trimode Ethernet MAC core, UART controller, I2C controller etc. Processor application code is complied and stored in the Block Memories, which are integral part of any FPGA. This avoids the need for external memory components. MicroBlaze processor provides connectivity with external world over Ethernet interface. UART connectivity is also provided for debug purpose. Commands received over the Ethernet interface are parsed and appropriate settings are made to the control registers to achieve desired functionality. The type of waveform to be generated is configurable on-the-fly by user. Also, the board status is monitored for health parameters such as voltages and temperature and is reported periodically to the host controller.

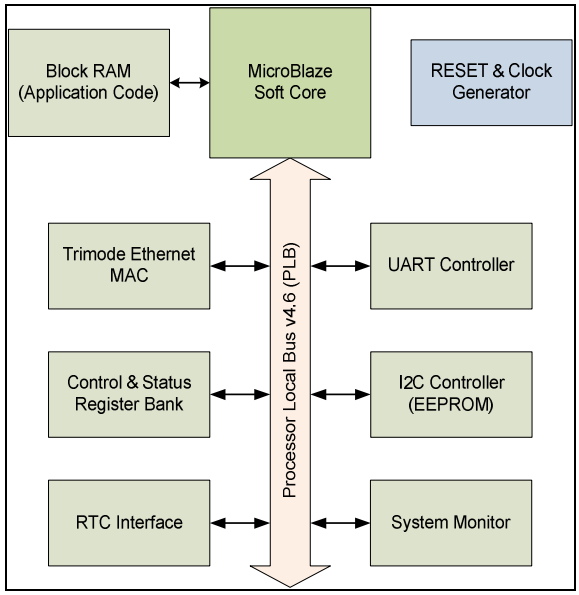

Figure 3: Representative embedded processor sub-system

VI. High Speed Design Challenges

Higher sampling rate of DAC resulted in an increase in the design complexity in terms of FPGA RTL design as well as high speed PCB design. Data interface from FPGA to the DAC is 48-bit, four 12-bit samples. Since the DAC is sampled at 2 GSPS, data from FPGA shall be transferred at 500 MHz SDR or 250 MHz DDR. Current implementation transferred data to the DAC using 48 differential lines each operating at 250 MHz LVDS DDR. All these lines have to be aligned on-board such that data on all the lines reaches DAC at the same time, which puts tighter constraints on the length matching requirements on the PCB. All these differential routes are length matched on the board to a tolerance of 200 mils.

FPGAs too have internal routing delays, which can significantly impact the signal timings. Therefore, FPGA internal logic needs to drive data onto all the DAC interface pins at the same time. A mismatch in the digital data arrival time at the DAC might lead to the incorrect sampling by the DAC and thereby design failure. This is achieved by clocking all the signals from the FPGA to the DAC in the input output blocks (IOBs) of Xilinx FPGA [3]. Clocking a signal in the IOB moves it closure to the FPGA pad and ensures that internal routing delays in the FPGA do not affect the overall design performance.

As the DAC sampling clock is 2 GSPS, the maximum signal frequency generated by the DAC is limited to 600 MHz in the present work. Clock circuitry driving 2 GHz clock to the DAC is to be properly shielded, so that it does not get affected by other areas of the design, while at the same time it should not affect other sections on-board. Similar argument holds good for analog output of the DAC. Traditional PWB layout design techniques no longer work at GHz speeds. The complexity level increases further as both digital and analog components are part of the same PCB, which requires isolating analog section from the digital section. Therefore, 2 GHz clock and high speed analog signals are shielded in such a way that interference from adjacent signals on the same layer or the layers below is minimized. This is accomplished by following Grounded Coplanar Wave Guide (CPWG) as the transmission line method for high speed signals. Figure 4 depicts a typical CPWG cross section. Here, via holes connect the lateral ground planes on the top side of the wafer to bottom side.

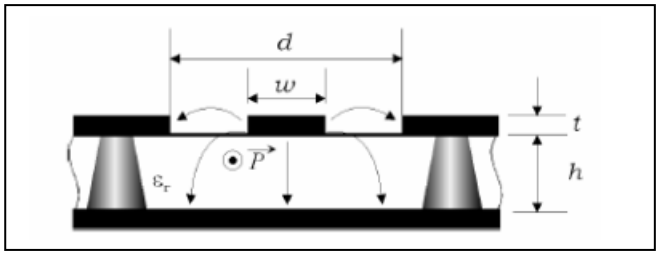

Figure 4: CPWG Cross-Section

Also, signal integrity problems are minimized by – keeping the traces as straight as possible, having a maximum of 2 via

in the signal path, using arc shaped traces instead of right-angles bends as shown in Figure 5.

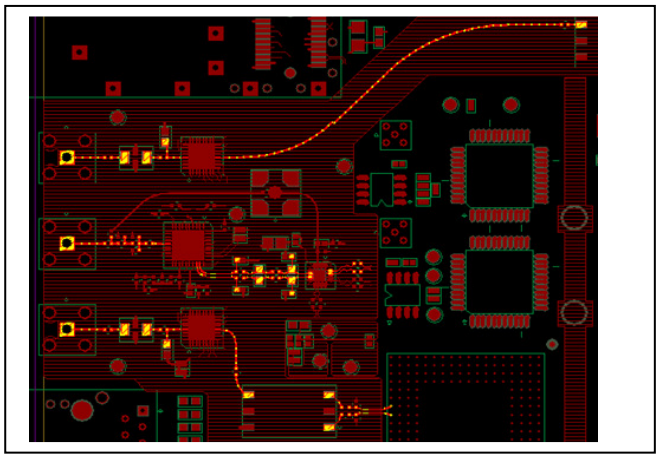

Figure 5: Arc shaped Signal Routing

VII. Mixed Signal Design Aspects

Combining High Speed Digital and Analog Signal circuits into a Small form Factor Solution requires special care during Board design and Layout. Noise reduction on a Mixed Signal board is to start from the Digital Section.

FPGAs can generate supply/ground bounce when switching at high frequencies. Supply and ground bounce are taken care of by reducing the simultaneously switching outputs (SSO), spreading SSO pins, using low slew rate signals, proper decoupling of power supply pins and by using series terminations wherever possible.

All high speed interfaces on board are terminated properly. Any transmission line will result in reflection if not terminated properly. Wherever possible, low noise I/O standards like LVDS are used. All high speed signals have a continuous solid reference plane below it, as discontinuity in reference plane can lead to increased crosstalk, reflections and EMI.

Digital and Analog circuits on-board are carefully partitioned. The component placement is done in such a way that stray digital current are not allowed to pass through the analog section to the extent possible.

Majority of the DACs require low impedance connection between its AGND and DGND pins. To provide this low impedance path, the AGND and DGND are shorted below the DAC. PCB layout is done in such a way that all data lines to the DAC see a solid reference plane. The Analog section is shielded by placing ground vias. Enough ground vias are staggered in the analog section to act like a solid ground plane.

Star topology is used to route power to the Analog section. The Digital power section is placed away from the analog power to avoid coupling of DC-DC switching noise to the analog supply. The Moats on ground plane around the AGND ensure that no return path exist for the digital signal. Input voltage to the LDO is filtered to remove SMPS switching noise. A DC-DC pre-regulation stage is provided to enhance the efficiency of the analog power section and to reduce the heat dissipation. Figure 6 shows how the analog and digital sections are isolated on-board.

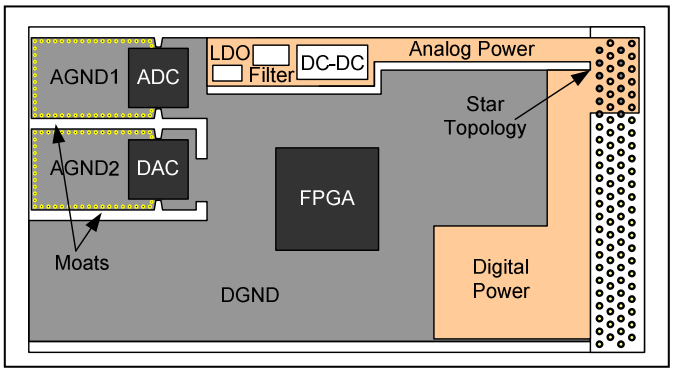

Figure 6: Isolation between Digital and Analog Supply

VIII. Conclusions

Baseband Generator has been tested extensively in the lab for generation of various types of waveforms discussed above and the results have met the design specifications in terms of functionality and output power levels. SFDR achieved on the board is -50 dBc at 600 MHz, while datasheet specification is -52 dBc. Phase Noise performance achieved on-board is –104 dBc/Hz at 1 KHz offset. This holds a great promise for future RADAR systems as it provides enhanced performance capabilities.

As is true for most of the military applications, it is difficult to determine for Electronic Warfare applications too whether the requirement for more processing power is driving the need for powerful hardware, software and RTL, or whether the designers in the related areas are proactive in identifying the opportunities and coming up with new ideas as and when a powerful hardware, software or Integrated circuit is released in the market. Programmability however is the driving force, so that a common hardware platform can be used for a wide variety of applications by modifying the software and/or RTL components. In a nut shell, today's RADAR systems are dependent on 3 key factors – more processing power, programmability & scalability, and ease of use. Application demands have outpaced the processor's ability to deliver, and that's where the FPGA's offer tremendous processing potential. They can support pipeline structures of variable depth and provide parallel computing resources, allowing even highly complex functions to be implemented with single-clock cycle execution. The programmability of FPGAs ensures that they can be tuned to meet the specific needs of an application without changing the hardware platform. Also, with the growing requirements for scalability, the need to adapt to constantly changing applications and the necessity of launching new applications as rapidly as possible, FPGA based implementations have come out handy because of its ease of use, and simultaneously providing important improvements in developer's productivity.

Xilinx Virtex-5 FPGAs have proven to be a success for Baseband Generator in terms of computational power. The release of Virtex-7 family and especially the Zync series with ARM processors holds greater scope for improvements and enhanced capabilities due to even faster data rates, higher processing resources, lower power consumption and hence improved thermal management. Virtex-7 FPGA based solution would prove to be cost effective too.

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