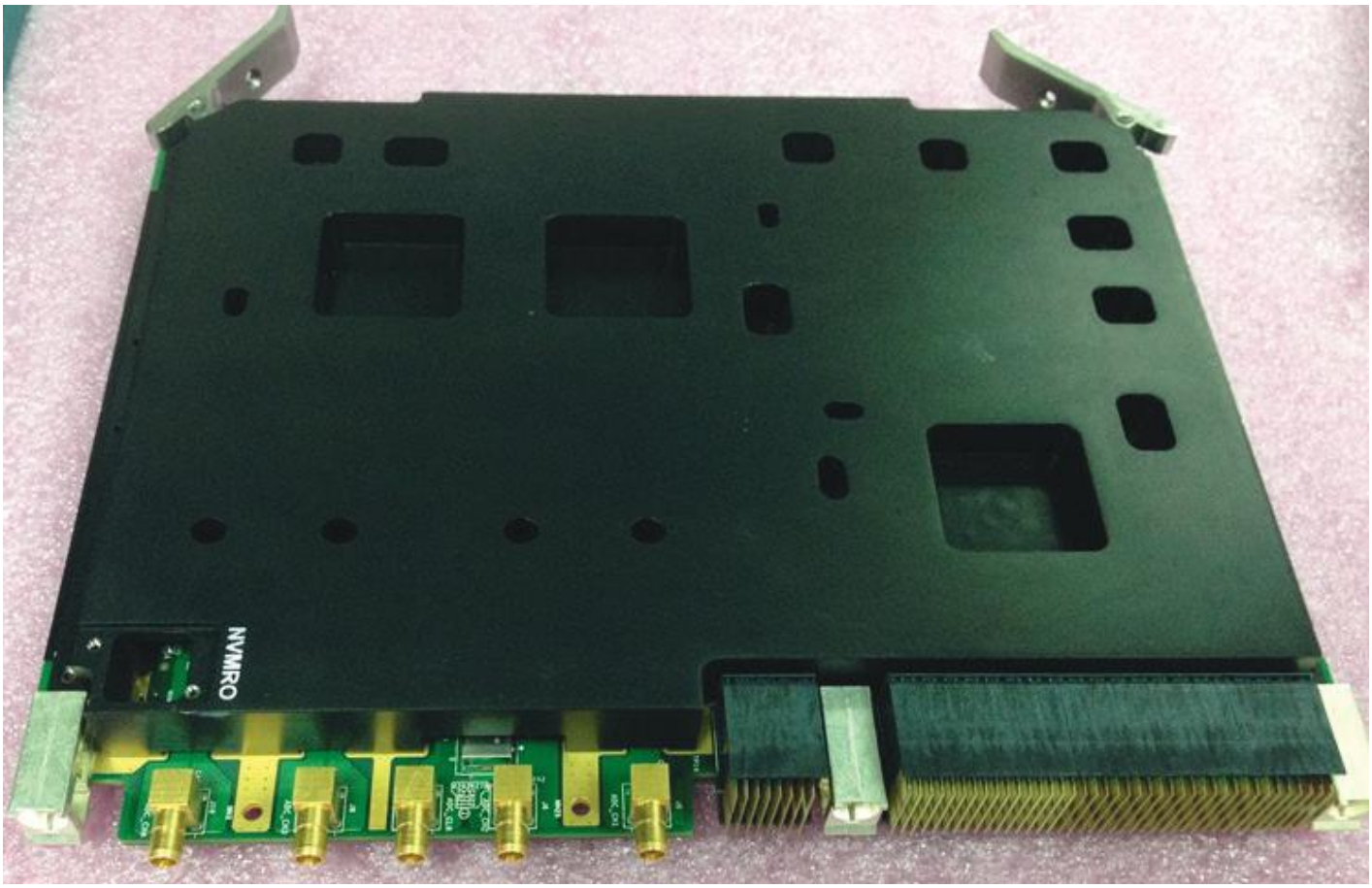
CoreEL Technologies
Enabling Excellence

Digital Intermediate Frequency (DIF) ReceiverBoard

Digital Intermediate Frequency (DIF) receiver board is a FPGA based high speed data acquisition board. High speed ADCs are used for digitization of analog IF signals and Virtex-5 series FPGAs for front-end digital signal processing and data streaming over high speed links. The board receives four channel analog signals for digitization. The required timing signals are fed from radar timing and IO generation board. FPGA based solution is implemented to meet the functional requirements of the board.

The DIF receiver board finds application in multiple airborne radar platforms:

- Exciter Receiver Processor
- Radar Processing Unit



KEY FEATURES

- Data acquisition and signal processing on the same platform
- Blind mate RF connection which mates to custom VPX Backplane.
- Four 16 bit ADCs sampling at 160MHz
- Time synchronously sampling at the four ADCs
- Remote FPGA programming support via LAN
- Board health monitoring over I2C interface

SPECIFICATIONS

FPGAs/Processor

- One Virtex-5 FX100T used for external data transfer and communication
- Two Virtex-5 SX95T FPGA used for ADC interface and implementation of Signal processing functions
- Four onboard 16 bit, 160 MSPS ADCs with Dynamic range 2.25Vp-p and 50 ohms impedance, two each inter faced to SX FPGAs

ADC IF input

- SNR: SNR>64 dBFS @Fin=70 MHz, Fs = 160 MHz
  SNR>58 dBFS @Fin=200 MHz, Fs = 160 MHz
- SFDR: SFDR>80 dBc @Fin=70 MHz, Fs = 160 MHz
  SFDR>72 dBc @Fin=200 MHz, Fs = 160 MHz

Interfaces

- sRIO interface: Two x4 sRIO interfaces for communication through backplane for high-speed data transfer from DIF card operating at 3.125Gbps
- Two sFPDP interface operating at 2.5 Gbps through backplane for data transfer from DIF board to external system
- Ethernet interface: Ethernet interface is provided for communication with remote host systems. The PPC based embedded sub-system implements the necessary software stack.

Software

- Control, Configuration and Status monitoring
- MicroBlaze based embedded processor with peripherals such as boot memory, system monitor, timer module, UART, Interrupt controller etc. on Virtex 5 SX FPGA.
- Power PC based embedded processor with peripherals such as boot memory, system monitor, timer module, UART, Interrupt controller etc. on Virtex 5 FX FPGA.

Additional information

- 512MB DDR2 SDRAM on each FPGA
- 256MB (32-bit) NOR FLASH memory on each FPGA
- Clock synthesizer for functioning of the PPC440 processor embedded in the Virtex 5 FX FPGA and Microblaze processor embedded in Virtex 5 SX FPGA

MECHANICAL

- Conduction cooled 6U custom VPX form factor with Blind mate RF connection which mates to custom VPX Backplane.
- The board weighs 1.45kg

POWER CONSUMPTION

- The boardconsumesa maximum of 55 W power
- Input voltages is 12V and 5V as per VPX standard

ENVIRONMENTAL

- Qualification : MIL-STD810D
  EMI/EMC MIL-STD-461E
  ESS: MIL-STD-2164 (EC)

- Temperature range : –40°C and +85°C (Storage)
  –40°C and +55°C (Operational)

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